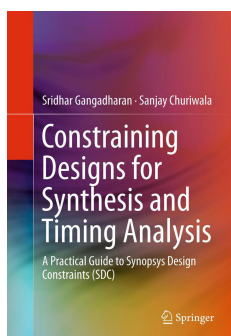


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## CONSTRAINING DESIGNS FOR SYNTHESIS AND TIMING ANALYSIS EBOOKS 2019



Author: Sridhar Gangadharan u0026 Sanjay Churiwala

Release Date: Lanzamiento previsto: @@expectedReleaseDate@@

This book serves as a hands-on guide to timing constraints in integrated circuit design.u0026#xa0; Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly.u0026#xa0; Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing.u0026#xa0; Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.u003cbr /u003eu003cbr /u003eu0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0; Provides a hands-on guide to synthesis and timing analysis, using Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints;u003cbr /u003eu003cbr /u003eu0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0; Includes key topics of interest to a synthesis, static timing analysis oru0026#xa0; place and route engineer;u003cbr /u003eu003cbr

/u003e-u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0; Explains which constraints command to use for ease of maintenance and reuse, given several options possible to achieve the same effect on timing;u003cbr /u003eu003cbr

/u003e-u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0;u0026#xa0; Explains fundamental concepts and provides exact command syntax.

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